AFFILIATED INSTITUTIONS
ANNA UNIVERSITY, CHENNAI
REGULATIONS - 2009
CURRICULUM II TO IV SEMESTERS (FULL TIME)
M.E. APPLIED ELECTRONICS

SEMESTER II

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<thead>
<tr>
<th>SL. NO</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AP9221</td>
<td>Analysis and Design of Analog Integrated Circuits</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>AP9222</td>
<td>Computer Architecture and Parallel Processing</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>AP9223</td>
<td>Digital Control Engineering</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>AP9224</td>
<td>Embedded Systems</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>E2</td>
<td>Elective II</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>E3</td>
<td>Elective III</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>

PRACTICAL

<table>
<thead>
<tr>
<th>SL. NO</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>L</th>
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<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>AP9227</td>
<td>Electronics Design Lab II</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>2</td>
</tr>
</tbody>
</table>

TOTAL 18 0 4 20

SEMESTER III

<table>
<thead>
<tr>
<th>SL. NO</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>E4</td>
<td>Elective IV</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>E5</td>
<td>Elective V</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>E6</td>
<td>Elective VI</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>

PRACTICAL

<table>
<thead>
<tr>
<th>SL. NO</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>AP9234</td>
<td>Project Work (Phase I)</td>
<td>0</td>
<td>0</td>
<td>12</td>
<td>6</td>
</tr>
</tbody>
</table>

TOTAL 9 0 12 15

SEMESTER IV

<table>
<thead>
<tr>
<th>SL. NO</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Project Work (Phase II)</td>
<td>0</td>
<td>0</td>
<td>24</td>
<td>12</td>
</tr>
</tbody>
</table>

TOTAL 0 0 24 12

Total no.of credits to be earned for the award of Degree 21+20+15+12 = 68
# LIST OF ELECTIVES

**M.E. APPLIED ELECTRONICS**

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<thead>
<tr>
<th>SL. NO</th>
<th>COURSE CODE</th>
<th>COURSE TITLE</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AP9251</td>
<td>Digital Image Processing</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>AP9252</td>
<td>Neural Networks and Its Applications</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>AP9253</td>
<td>Robotics</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>VL9211</td>
<td>DSP Integrated Circuits</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>VL9261</td>
<td>ASIC Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>AP9260</td>
<td>Design and Analysis of Algorithms</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>7</td>
<td>NE9251</td>
<td>Reliability Engineering</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>8</td>
<td>AP9256</td>
<td>Electromagnetic Interference and Compatibility in System Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>9</td>
<td>CP9212</td>
<td>High Performance Computer Networks</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>10</td>
<td>AP9258</td>
<td>RF system Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>11</td>
<td>VL9252</td>
<td>Low Power VLSI Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>12</td>
<td>VL9253</td>
<td>VLSI Signal Processing</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>13</td>
<td>VL9254</td>
<td>Analog VLSI Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>14</td>
<td>VL9221</td>
<td>CAD for VLSI Circuits</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>15</td>
<td>AP9259</td>
<td>Hardware Software Co-design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>16</td>
<td></td>
<td>Special Elective</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>
UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES

UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC
Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references. Output stages: Emitter follower, source follower and Push pull output stages.

UNIT III OPERATIONAL AMPLIFIERS
Analysis of operational amplifiers circuit, slew rate model and high frequency analysis, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise

UNIT IV ANALOG MULTIPLIER AND PLL
Analysis of four quadrant and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY
MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic- Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers

TOTAL: 45PERIODS

REFERENCES:

2. Behzad Razavi, “Principles of data conversion system design”, S.Chand and company Ltd, 2000
UNIT I  THEORY OF PARALLELISM  9
Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties - Conditions of parallelism.

UNIT II  PARTITIONING AND SCHEDULING  9
Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance - performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

UNIT III  HARDWARE TECHNOLOGIES  9
Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory - backplane bus systems, cache memory organisations, shared memory organisations, sequential and weak consistency models.

UNIT IV  PIPELINING AND SUPERSCALAR TECHNOLOGIES  9
Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V  SOFTWARE AND PARALLEL PROGRAMMING  9
Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TOTAL: 45 PERIODS

REFERENCES:
UNIT I PRINCIPLES OF CONTROLLERS
Review of frequency and time response analysis and specifications of control systems, need for controllers, continues time compensations, continues time PI, PD, PID controllers, digital PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL
Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM
Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS
Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS
Algorithm development of PID control algorithms, software implementation, implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

TOTAL: 45 PERIODS

REFERENCES:
UNIT I  EMBEDDED PROCESSORS

UNIT II  EMBEDDED PROCESSOR AND COMPUTING PLATFORM
Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock. Hybrid Architecture

UNIT III  NETWORKS
Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV  REAL-TIME CHARACTERISTICS

UNIT V  SYSTEM DESIGN TECHNIQUES

TOTAL: 45 PERIODS

REFERENCES:
AP9227 ELECTRONICS DESIGN LAB II  L T P C  0 0 4 2

1. System design using PLL
2. System design using CPLD
3. Alarm clock using embedded micro controller
4. Model train controller using embedded micro controller
5. Elevator controller using embedded micro controller
6. Simulation of Non adaptive Digital Control System using MAT LAB control system toolbox
7. Simulation of Adaptive Digital Control System using MAT LAB control system toolbox

AP9251 DIGITAL IMAGE PROCESSING  L T P C  3 0 0 3

UNIT I  DIGITAL IMAGE FUNDAMENTALS  9
Elements of digital image processing systems, Vidicon and Digital Camera working principles, Elements of visual perception, brightness, contrast, hue, saturation, Mach Band effect, Image sampling, Quantization, Dither, Two dimensional mathematical preliminaries.

UNIT II  IMAGE TRANSFORMS  9
1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

UNIT III  IMAGE ENHANCEMENT AND RESTORATION  9

UNIT IV  IMAGE SEGMENTATION AND RECOGNITION  9
Image segmentation - Edge detection, Edge linking and boundary detection, Region growing, Region splitting and Merging, Image Recognition - Patterns and pattern classes, Matching by minimum distance classifier, Matching by correlation., Neural networks-Backpropagation network and training, Neural network to recognize shapes.

UNIT V  IMAGE COMPRESSION  9
Need for data compression, Huffman, Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding, Transform coding, JPEG standard, JPEG 2000, EZW, SPIHT, MPEG.

TOTAL: 45 PERIODS
REFERENCES:


AP9252 NEURAL NETWORKS AND ITS APPLICATIONS

UNIT I BASIC LEARNING ALGORITHMS

UNIT II RADIAL-BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES

UNIT III COMMITTEE MACHINES

NEURODYNAMICS SYSTEMS
UNIT IV ATTRACTION NEURAL NETWORKS

- Associative Learning – Attractor Neural Network
- Associative Memory – Hopfield Network
- Content Addressable Memory – Strange Attractors and Chaos
- Error Performance of Hopfield Networks – Applications of Hopfield Networks
- Simulated Annealing – Boltzmann Machine – Bidirectional Associative Memory
- BAM Stability Analysis – Error Correction in BAMs – Memory Annihilation of Structured Maps in BAMS
- Continuous BAMs – Adaptive BAMs

ADAPTIVE RESONANCE THEORY


UNIT V SELF ORGANISING MAPS

- Self-organizing Map
- Maximal Eigenvector Filtering – Sanger’s Rule – Generalized Learning Law – Competitive Learning
- Vector Quantization – Mexican Hat Networks – Self-organizing Feature Maps – Applications

PULSED NEURON MODELS

- Spiking Neuron Model
- Integrate-and-Fire Neurons
- Conductance Based Models – Computing with Spiking Neurons

TOTAL: 45 PERIODS

REFERENCES:


AP9253 ROBOTICS L T P C

3 0 0 3

UNIT I INTRODUCTION TO ROBOTICS

- Motion - Potential Function, Road maps, Cell decomposition and Sensor and sensor planning
- Kinematics. Forward and Inverse Kinematics - Transformation matrix and DH transformation. Inverse Kinematics - Geometric methods and Algebraic methods

Non-Holonomic constraints
UNIT II  COMPUTER VISION  9

UNIT III  SENSORS AND SENSING DEVICES  9

UNIT IV  ARTIFICIAL INTELLIGENCE  9

UNIT V  INTEGRATION TO ROBOT  9
Building of 4 axis or 6 axis robot - Vision System for pattern detection - Sensors for obstacle detection - AI algorithms for path finding and decision making.

TOTAL: 45 PERIODS

REFERENCES:

VL9211  DSP INTEGRATED CIRCUITS  L T P C
3 0 0 3

UNIT I  DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES  9
Standard digital signal processors, Application specific IC’s for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

UNIT II  DIGITAL SIGNAL PROCESSING  9
UNIT III  DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS  
FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT IV  DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES  
DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit - serial PEs.

UNIT V  ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN  
Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. Cordic algorithm.

REFERENCES:
UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING
Verilog and logic synthesis - VHDL and logic synthesis - types of simulation - boundary scan test - fault simulation - automatic test pattern generation.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING
System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow – global routing - detailed routing - special routing - circuit extraction - DRC.

REFERENCES:

TOTAL: 45 PERIODS
REFERENCES:


NE9251 RELIABILITY ENGINEERING L T P C 3 0 0 3

UNIT I PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE 9
Statistical distribution, statistical confidence and hypothesis testing, probability plotting techniques – Weibull, extreme value, hazard, binomial data; Analysis of load – strength interference, Safety margin and loading roughness on reliability.

UNIT II RELIABILITY PREDICTION, MODELLING AND DESIGN 9
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis, Petrick Nets, State space Analysis, Monte Carlo simulation, Design analysis methods – Quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY 9
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV RELIABILITY TESTING AND ANALYSIS 9
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V MANUFACTURE AND RELIABILITY MANAGEMENT 9
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

TOTAL: 45 PERIODS
REFERENCES:


AP9256 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN

UNIT I   EMI/EMC CONCEPTS 3003
EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II   EMI COUPLING PRINCIPLES 9
Conducted, radiated and transient coupling; Common ground impedance coupling; Common mode and ground loop coupling; Differential mode coupling; Near field cable to cable coupling, cross talk; Field to cable coupling; Power mains and Power supply coupling.

UNIT III   EMI CONTROL TECHNIQUES 9
Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV   EMC DESIGN OF PCBS 9
Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V   EMI MEASUREMENTS AND STANDARDS 9
Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL: 45 PERIODS

REFERENCES:

UNIT I  INTRODUCTION
Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing.
SONET – DWDM – DSL – ISDN – BISDN, ATM.

UNIT II  MULTIMEDIA NETWORKING APPLICATIONS
Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.

UNIT III  ADVANCED NETWORKS CONCEPTS

UNIT IV  TRAFFIC MODELLING
Little’s theorem, Need for modeling, Poisson modeling and its failure, Non-poisson models, Network performance evaluation.

UNIT V  NETWORK SECURITY AND MANAGEMENT

TOTAL:45 PERIODS

REFERENCES:
UNIT I  CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES
CMOS: Introduction to MOSFET Physics – Noise: Thermal, shot, flicker, popcorn noise
Transceiver Specifications: Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link
Transceiver Architectures – Receiver: Homodyne, Heterodyne, Image reject, Low IF Architectures – Transmitter: Direct up conversion, Two step upconversion

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS
S-parameters with Smith chart – Passive IC components - Impedance matching networks Amplifiers: Common Gate, Common Source Amplifiers – OC Time constants in bandwidth estimation and enhancement – High frequency amplifier design

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS
Feedback Systems: Stability of feedback systems: Gain and phase margin, Root-locus techniques – Time and Frequency domain considerations – Compensation

UNIT IV PLL AND FREQUENCY SYNTHESIZERS
PLL: Linearised Model – Noise properties – Phase detectors – Loop filters and Charge pumps Frequency Synthesizers: Integer-N frequency synthesizers – Direct Digital Frequency synthesizers

UNIT V MIXERS AND OSCILLATORS
Mixer: characteristics – Non-linear based mixers: Quadratic mixers – Multiplier based mixers: Single balanced and double balanced mixers – subsampling mixers
Oscillators: Describing Functions, Colpitts oscillators – Resonators – Tuned Oscillators – Negative resistance oscillators – Phase noise

TOTAL: 45 PERIODS

TEXT BOOKS:
UNIT I  POWER DISSIPATION IN CMOS  9
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.

UNIT II  POWER OPTIMIZATION  9
Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers.

UNIT III  DESIGN OF LOW POWER CMOS CIRCUITS  9
Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques

UNIT IV  POWER ESTIMATION  9
Power estimation techniques – Logic level power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V  SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER  9
Synthesis for low power –Behavioral level transforms- Software design for low power -

TOTAL : 45 PERIODS

REFERENCES:

2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, DESIGNING CMOS CIRCUITS FOR LOW POWER, Kluwer,2002

UNIT I  INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS  9
Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.
UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS

UNIT IV SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING

TOTAL : 45 PERIODS

REFERENCES:

VL9254 ANALOG VLSI DESIGN L T P C
3 0 0 3

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING
UNIT II  BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT-MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING  9
Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III  SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS  9

UNIT IV  DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS  9

UNIT V  STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT  9

TOTAL : 45 PERIODS

REFERENCES:

VL9221  CAD FOR VLSI CIRCUITS  L T P C
3 0 0 3

UNIT I  VLSI DESIGN METHODOLOGIES  9
UNIT II DESIGN RULES
Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT III FLOOR PLANNING
Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION
Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V MODELLING AND SYNTHESIS

TOTAL: 45 PERIODS

REFERENCES:
UNIT IV PROTOTYPING AND EMULATION  9

UNIT V DESIGN SPECIFICATION AND VERIFICATION  9

TOTAL: 45 PERIODS

REFERENCES: