

## ABOUT THE INSTITUTE

Madras Institute of Technology is one of the premier technical institutions started in the year 1949 by Shri. C. Rajam, an eminent industrialist. The institute was the result of a bold experiment in technical education as it introduced for the first time, totally unconventional Engineering courses such as Aeronautical Engineering, Automobile Engineering, Electronics Engineering and Instrumentation Engineering. It was merged with Anna University in the year 1978.

## ABOUT THE DEPARTMENT

The Department of Electronics Engineering established in the year 1949, has its core strength in the leading areas of Electronics & Communication Technology. The academic programmes offered in the Department are B.E (Electronics and Communication Engineering), M.E (Communication and Networking) M.E (VLSI and Embedded Systems), M.E (Wireless Technologies). The cutting edge research areas include Embedded System design, VLSI Design Communication Technologies, Network Security, Sensor Networks, Optical Communication, Signal Processing, and Image Processing. The Department has collaborative partners from academia and industry both within India and worldwide.

## LOCATION

Madras Institute of Technology is located in Chrompet, Chennai and close to Chrompet railway station.

## ABOUT THE WORKSHOP

This course provides professors with an introduction to embedded system design flow on Zynq using ZedBoard and Xilinx Vivado® design software suite.

## WHO SHOULD ATTEND

Professors who are familiar with Xilinx All Programmable technology and wish to get up to speed with SoC-based embedded systems design using Zynq.

## Pre-requisites

- Digital logic and FPGA design experience
- Basic experience with Xilinx Vivado design software suite
- Basic understanding of C programming
- Basic microprocessor experience

## Course Overview

### Day 1:

• Introduction to Embedded System Design using Zynq

### Lab 1: Simple Hardware Design

- Create a Vivado project and use IP Integrator to develop a basic embedded system for a target board.
- Zynq Architecture
- Extending the Embedded System into Programmable Logic

### Lab 2: Adding Peripherals in Programmable Logic

- Extend the hardware system by adding AXI peripherals from the IP catalog
- Adding Your Own IP Peripheral

### Lab 3: Creating and Adding Your Own Custom IP

- Use the Manage IP feature of Vivado to create a custom IP and extend the system with the custom peripheral.

### Day 2:

## Software Development Environment

### Lab 4: Writing Basic Software Applications

- Write a basic C application to access the peripherals.
- Software Development and Debugging

### Lab 5: Software Debugging Using SDK

- Use API to drive CPU's timer. Perform software debugging using SDK.

## Course Outcomes

### you will be able to:

- Rapidly architect an embedded system targeting the ARM processor of Zynq located on ZedBoard using Vivado and IP Integrator
- Extend the hardware system with Xilinx provided peripherals
- Create a custom peripheral and add it to the system
- Write a software application to access peripherals
- Perform IP-level Bus Functional simulation verification

## RESOURCE PERSONS

- Experts from CoreEL Technologies.

## ABOUT THE REGISTRATION

- Number of seats is limited to 30.
- Registration Fee – Rs.1000/-
- DD should be taken in favor of The Dean, MIT Campus, Anna University.

Send the duly filled application along with DD to the Coordinator(s) by post.

## TARGETED PARTICIPANTS

- Participants from Industry and Academia (Faculty members and research scholars).

## REGISTRATION

1. Name :  
(in capital)
  2. Designation :
  3. Qualification :
  4. Department :
  5. Office Address :
  6. Phone (Office) :  
(Mobile) :
  7. DD No. and Bank :
  7. E-mail :
- Signature :

## CERTIFICATE FROM HEAD OF THE INSTITUTION

Dr./Mr./Mrs. \_\_\_\_\_ is an employee of our institution. He/She will be permitted to attend the programme if selected.

Signature of the Principal with seal  
**Last date of submission: 1/1/2018**  
**Intimation of selection: 3/1/2018**

## Embedded System Design Flow on Zynq using Vivado

**5<sup>th</sup> -6<sup>th</sup> January 2018**

**Convener**

**Dr.M.Kannan,  
Head of the Department,  
Dept of Electronics Engg.,**



**Coordinators**

**Dr.D.Meganathan  
Dr.V.Sathiesh Kumar**

*Organized by*

**Department of Electronics Engineering  
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Chennai – 600 044.**

**Contact:**

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