# DEPARTMENT OF ELECTRONICS ENGINEERING
# MIT CAMPUS, ANNA UNIVERSITY: CHENNAI - 600044
# ENGAGEMENT OF PROJECT ASSISTANT

## Notification for the Engagement of Project Assistant in the C2S project

**Adv. No.:** DEE/Project Assistant/C2S/2025/01

**Date:** 06.10.2025

Applications are invited from the eligible candidates for the **temporary post** of **"Project Assistant"** to be engaged in the Chip to Startup (C2S), MeitY, Govt. of India funded research project entitled **"ASIC Realization of Light Weight Hardware Security Protocol Architecture for RFID Enabled Applications"** at the Department of Electronics Engineering, MIT Campus, Anna University, Chennai.

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|---|---|
| Name of the Post | Project Assistant |
| No. of the Post(s) | 01 |
| Assistantship / Fellowship per month | ₹ 35,000/- (Consolidated) for 3 Years |
| Qualification | B.E.,/B.Tech., (ECE or any relevant domain) **or** M.E./M.Tech (VLSI Design/ Embedded System Technologies)<br>With minimum one year experience in FPGA implementation and Physical Design using Cadence or Synopsis EDA tools |

**General Instructions:**

1. Candidates should submit the application as per the given format in Annexure – I, along with a copy of self-attested degree certificates and other relevant documents.
2. Only shortlisted candidates will be called for the interview based on the eligibility criteria.
3. The date and time for the interview will be informed to the candidates through email.
4. Candidates should appear for the interview with their original certificates and other relevant documents.
5. The Assistantship is purely temporary and is subject to renewal of C2S Sanction.

6. Assistantship/ Fellowship will be paid as per the latest rules and guidelines of the C2S.
7. The position is purely contractual and temporary in nature, and will cease automatically as soon as project is completed/terminated.
8. Project will be carried out at MIT Campus, Anna University, Chennai.
9. No TA/DA will be provided to attend the interview.

**How to Apply:**

Interested candidates possessing qualifications, as stated above, may send their filled-in application (as per Annexure – I) by post and email ( vr_vijay@yahoo.com ) along with self-attested photocopies of educational qualifications, mark sheets, experience certificates (if applicable), evidence of other academic credentials, **on or before 27th October 2025 by 5.00 PM**. Kindly mention the project title **"ASIC Realization of Light Weight Hardware Security Protocol Architecture for RFID Enabled Applications"** in all your communications.

**Address for Correspondence:**

Dr. V.R.Vijaykumar (Principal Investigator),
Professor,
Department of Electronics Engineering,
MIT Campus, Anna University,
Chennai – 600 044.

6/10/25

Principal Investigator
(Dr.V.R.Vijaykumar)

Head of the Department
Department of EE

Head of Department
Department of Electronics Engineering
MIT CAMPUS, ANNA UNIVERSITY
CHROMEPET, CHENNAI - 600 044.

Annexure – I

**DEPARTMENT OF ELECTRONICS ENGINEERING**

**MADRAS INSTITUTE OF TECHNOLOGY CAMPUS**

**ANNA UNIVERSITY, CHENNAI - 600 044**

**No.:** DEE/Project Assistant/C2S/2025/01 **Date:** 06.10.2025

POST OF PROJECT ASSISTANT (TEMPORARY) - APPLICATION FORM

**Project Title: ASIC Realization of Light Weight Hardware Security Protocol Architecture for RFID Enabled Applications**

**(To be filled by office)**

| | | | |
|---|---|---|---|
| Application Number | | Date of Receipt of the application | |

**(To be filled by the applicant)**

**Personal Details:**

| | | | | |
|---|---|---|---|---|
| Full Name (In Capital) | | | | Affix Recent Passport Size Photo |
| Date of Birth (DD/MM/YY) | | Gender (Male/Female) | | |
| Marital Status (Married/Unmarried) | | Nationality | | |
| Category (Gen/BC/MBC/SC/ST) (Attach self-attested Photo copy of the certificate) | | | | |
| Address for Communication: | | Permanent Address: | | |
| Mobile/Phone No. | | E-mail ID | | |

**Education Background (from Matriculation to the highest qualification; Attach self-attested copies of the qualifying degree certificates and mark sheets)**

| S. No. | Qualification | Group/Branch/ Specialization | % Marks / CGPA & Class | Board / University | Year | Regular / Part time |
|---|---|---|---|---|---|---|
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**Qualifying Examination (GATE / CSIR-NET / UGC-NET / Others)**

| S. No. | Qualifying Examination | Branch | Year | Valid up to | Percentile | All India Rank | Any other information |
|---|---|---|---|---|---|---|---|
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**Professional Experience (Attach the self-attested copies of copies experience certificates)**

| S. No. | Designation | Name of Organization | Period | | Nature of Work |
|---|---|---|---|---|---|
| | | | From | To | |
| | | | | | |
| | | | | | |

Research Publications (if any, provide details) :
(Attach additional sheets if the space provided is insufficient)

Awards, Patents, Prizes etc., (if any, provide details) :
(Attach additional sheets if the space provided is insufficient)

Any other relevant information which is not covered above:
(Attach additional sheets if the space provided is insufficient)