



Centre for Academic Courses

Train-the-Trainer Program

# RTL to GDS II VLSI Design Flow Using Open Source EDA Tools

May 25<sup>th</sup> to 30<sup>th</sup>, 2026

Venue: Computer Lab, CEG, Anna University, Chennai



## Key Topics/Themes:

- Open-source EDA tool overview (e.g., OpenROAD, Magic, Yosys, graywolf)
- RTL synthesis and optimization
- Floorplanning and placement
- Floorplanning and placement strategies
- Clock tree synthesis (CTS) concepts
- Routing and timing closure
- Design rule checking (DRC) and layout versus schematic (LVS) verification
- Physical verification and GDS II stream out

Keynote Speakers/Resource Persons:  
VLSI Industry Experts

Target Audience:  
Faculties from Affiliated Colleges of Anna University

## Registration Details:



Deadline for Registration:  
**12<sup>th</sup> May 2026**

Registration link:  
<https://forms.gle/bjMAkqqtHghxC1Arz7>

Contact Person:

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